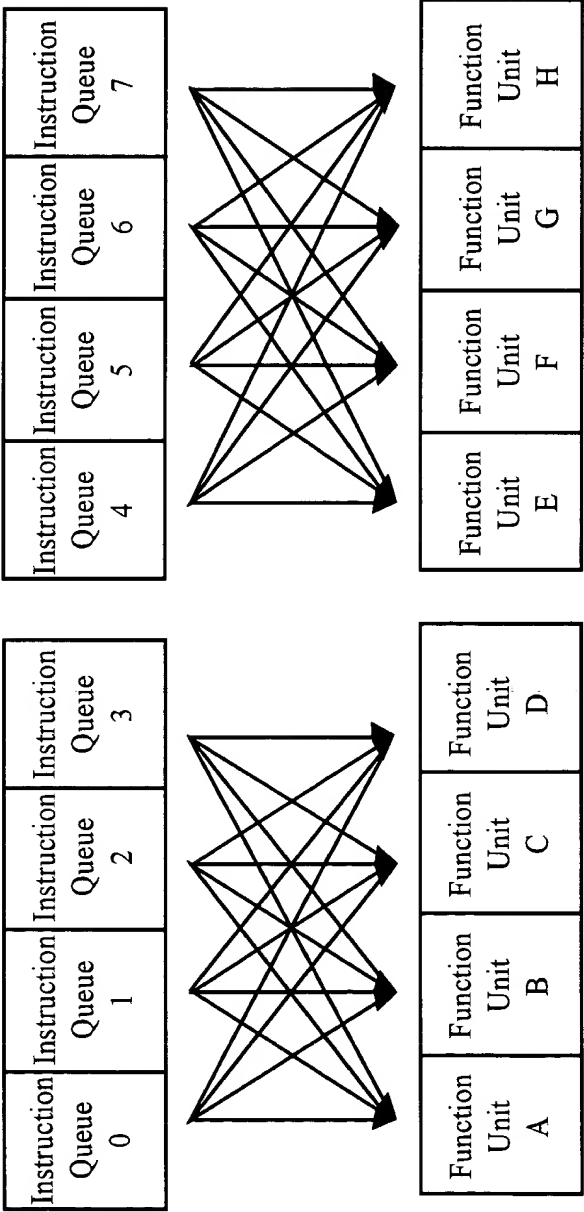


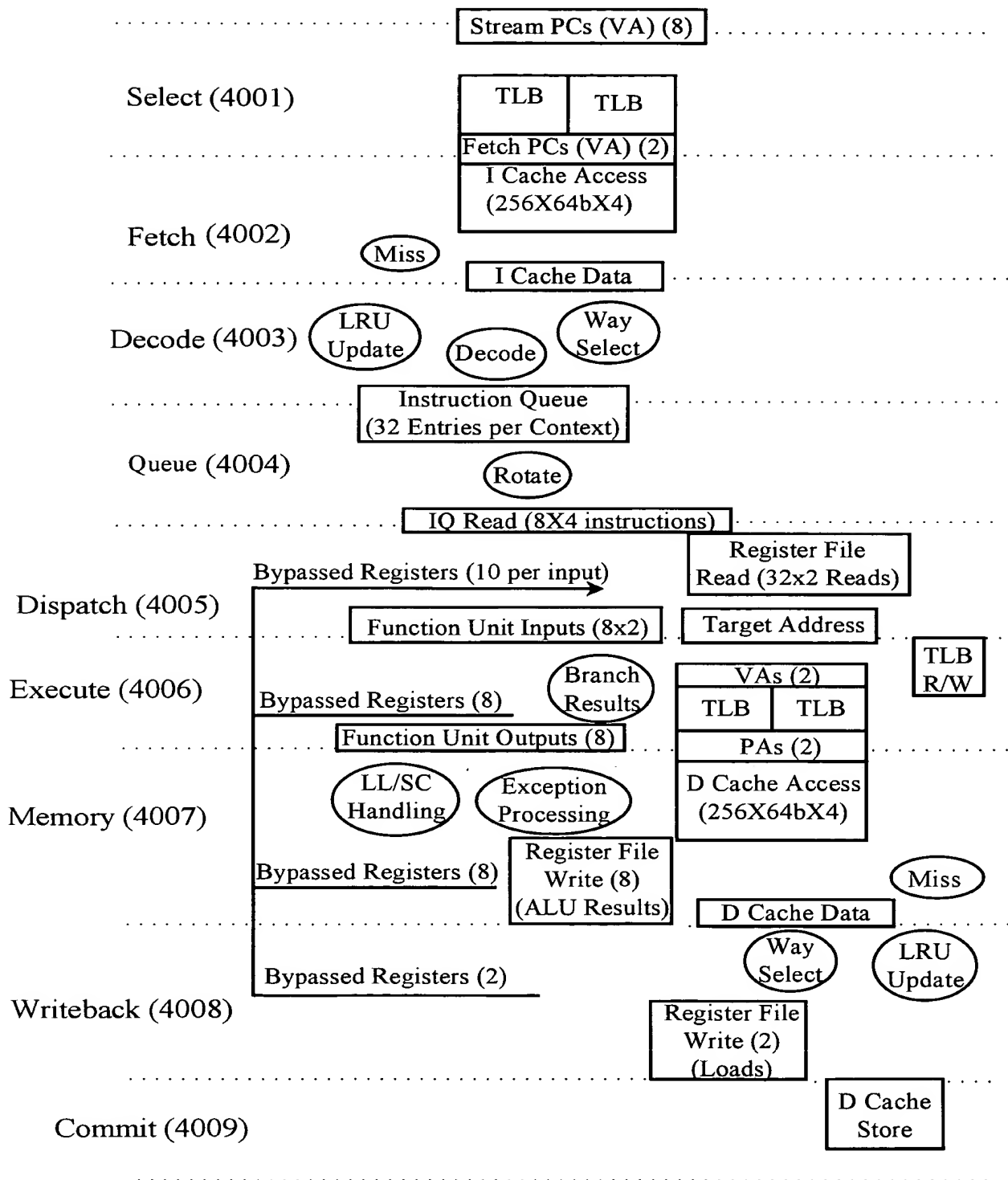
SPU Block Diagram

Fig. 1



Function Unit Dispatch Pattern

Fig. 3



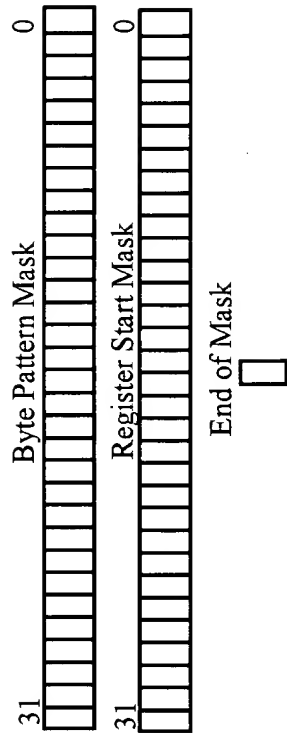
Pipeline Timing Diagram

Fig. 4

31	26	25	21	20	16	15	11	10	6	5	0
Special 0000000	RS	RT	MASK	LDX 00000	XSTREAM 110111						
Special 0000000	RS	RT	MASK	STX 00001	XSTREAM 110111						

Masked Load/Store Instructions

Fig. 5



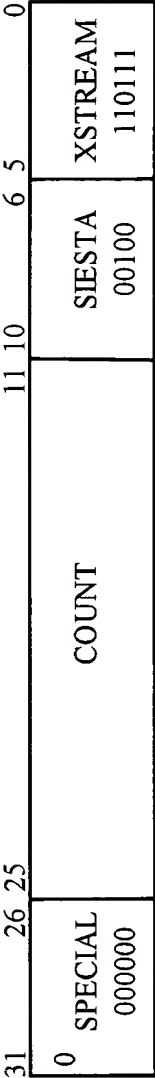
LDX/STX Mask Registers

Fig. 6

31	26	25	21	20	16	15	11	10	6	5	0
Special 0000000	RS	RT	RD	ADDX 00010	XSTREAM 110111						
Special 0000000	RS	RT	RD	SUBX 00011	XSTREAM 110111						

Special Arithmetic Instructions

Fig. 7



Siesta Instruction

Fig. 8

31	26	25	21	20	16	15	11	10	6	5	0
Special 0000000	RS	00000	RD	GETSPC 10000	XSTREAM 110111						
Special 0000000	RS	00000	00000	FREESPC 10001	XSTREAM 110111						

PMU - Packet Memory Instructions

Fig. 9

31	26	25	21	20	16	15	11	10	6	5	0
Special 0000000	RS		00000		00000		00000	PKTEXT 10010	XSTREAM 110111		
Special 0000000	RS		RT		RD			PKTINS 10011	XSTREAM 110111		
Special 0000000	RS		RT				00000	PKTDONE 10100	XSTREAM 110111		
Special 0000000	RS		RT				00000	PKTMOVE 10101	XSTREAM 110111		
Special 0000000	RS		RT				00000	PKTUPD 10110	XSTREAM 110111		
Special 0000000	RS		RT		ITEM			PKTPR 10111	XSTREAM 110111		
Special 0000000	RS		RT				00000	PKTMAR 11010	XSTREAM 110111		
Special 0000000	RS		000000		RD			PKTACT 11011	XSTREAM 110111		

PMU - Queuing System Instructions

Fig. 10

31	26 25	21 20	16 15	11 10	6 5	0
Special 0000000	00000	00000	00000	RELEASE 11000	XSTREAM 110111	
Special 0000000	RS	00000	RD	GETCTX 11001	XSTREAM 110111	

PMU - RTU Instructions

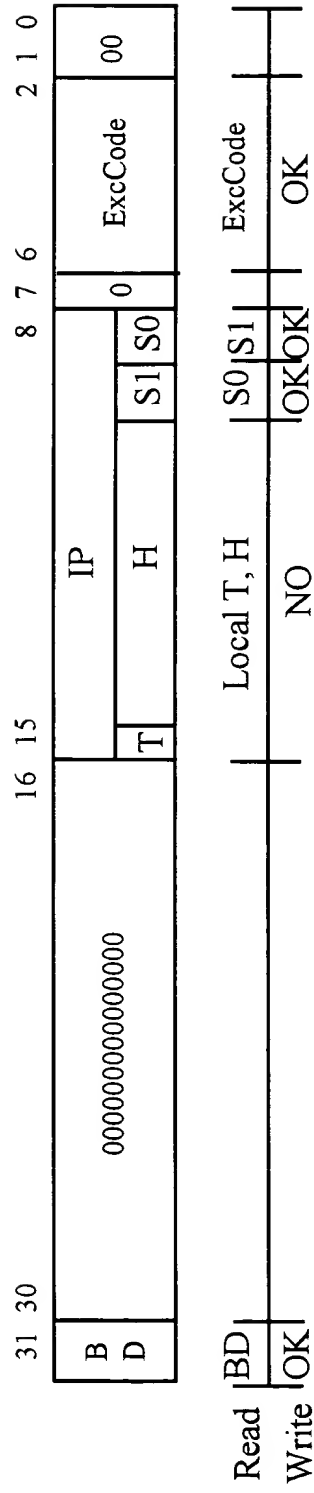
Fig. 11

31				29				27				23				16				15				8				7				5				4				3				2				1				0															
000				C				U				0				B				E				V				000000				000000				IM				000				KSU				0				E				X				L				IE			

Status Register

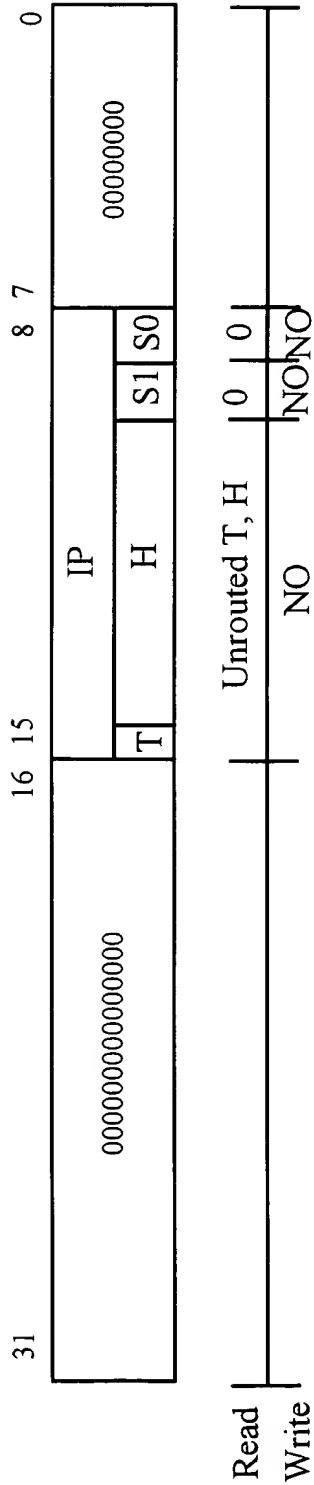
Fig. 13

00000000000000000000000000000000



Cause Register

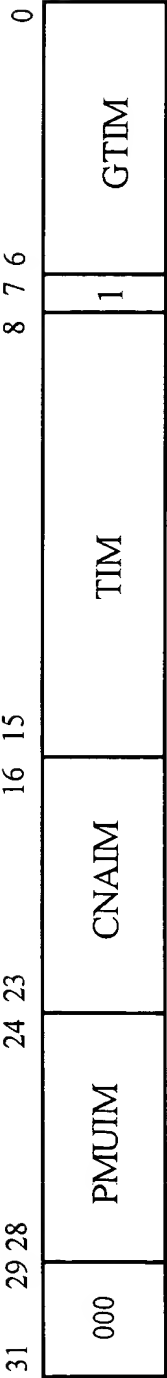
Fig. 14



Global Cause Register

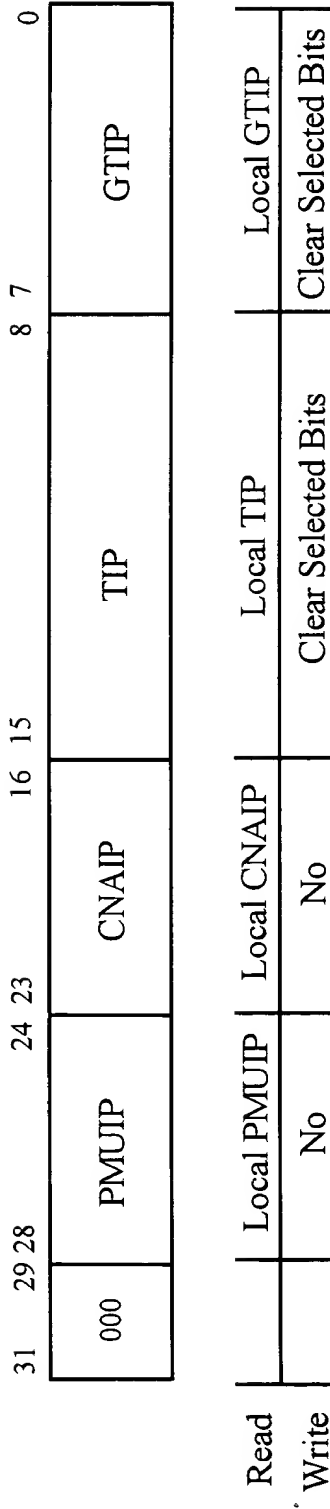
Fig. 15

000000000000000000000000



Extended Interrupt Mask Register

Fig. 16



Extended Interrupt Pending Register

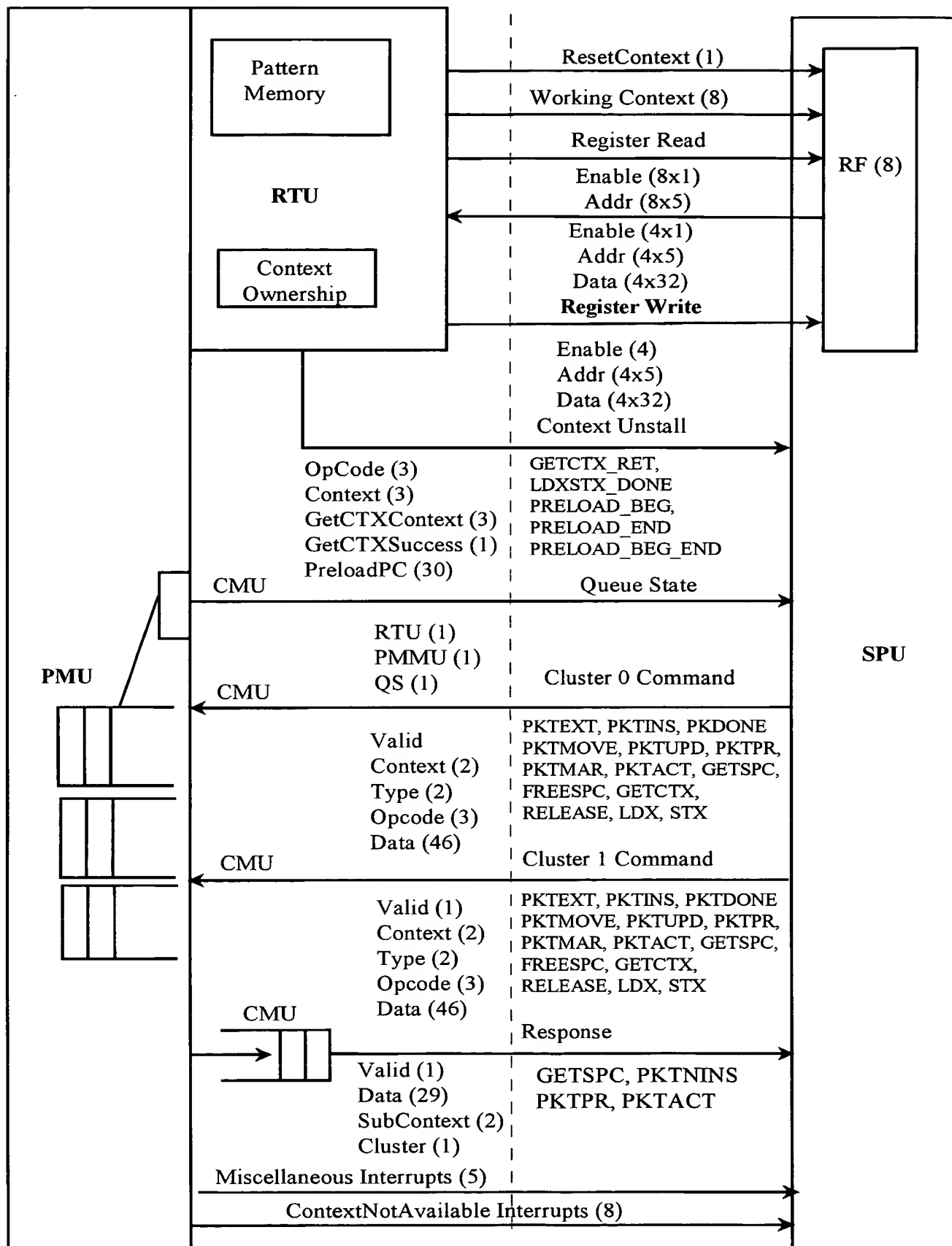
Fig. 17

31	29	28	24	23	16	15	8	7	0			
000			PMUIP			CNAIP			TIP		GTIP	

Read Write	Unrouted PMUIP		Unrouted CNAIP		Unrouted TIP		00000000	
	No		No		Deliver Selected Interrupts		Deliver Selected Interrupts	

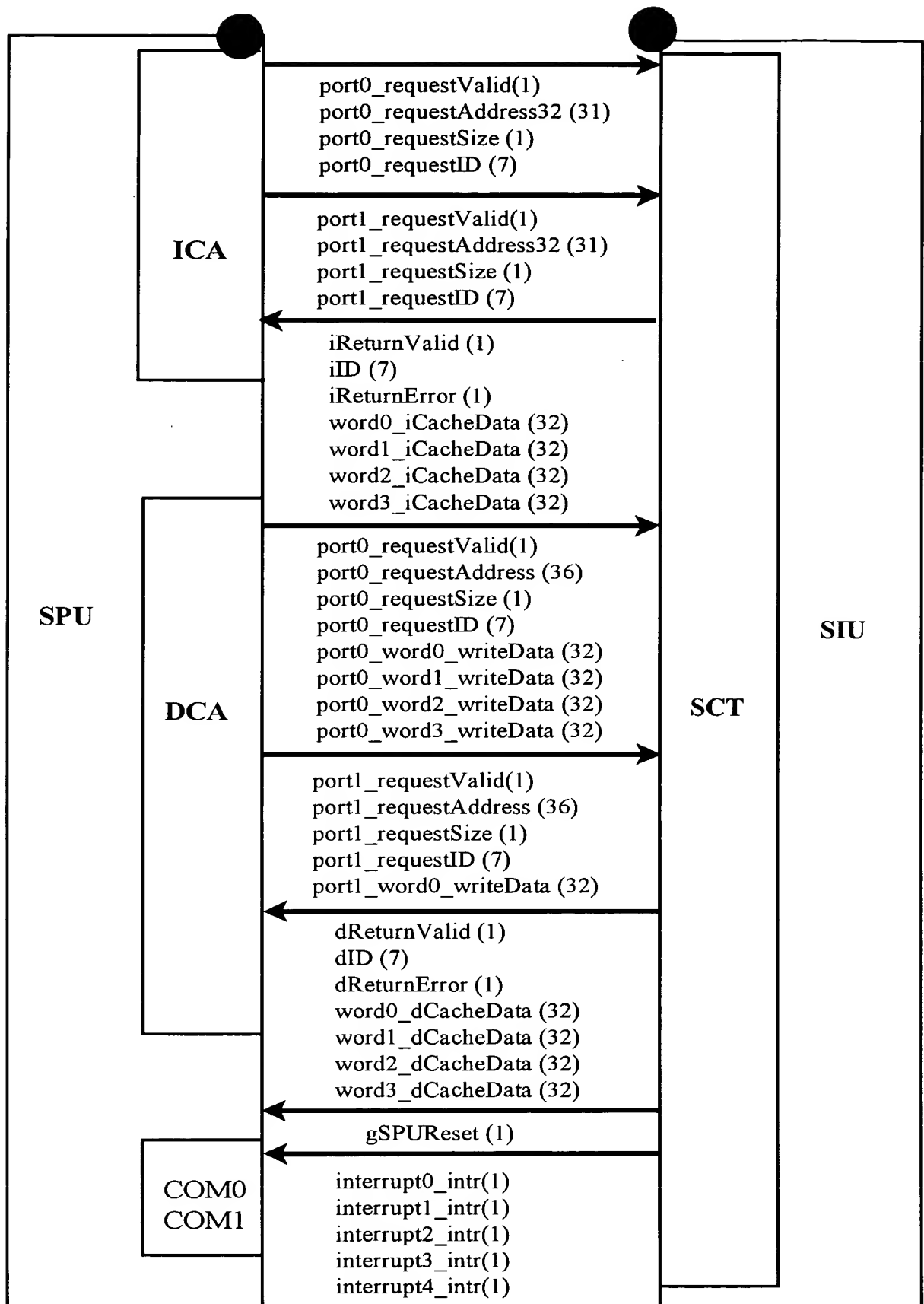
Global Extended Interrupt Pending Register

Fig. 18



PMU/SPU Interface

Fig. 19



SIU/SPU Interface

Fig. 20

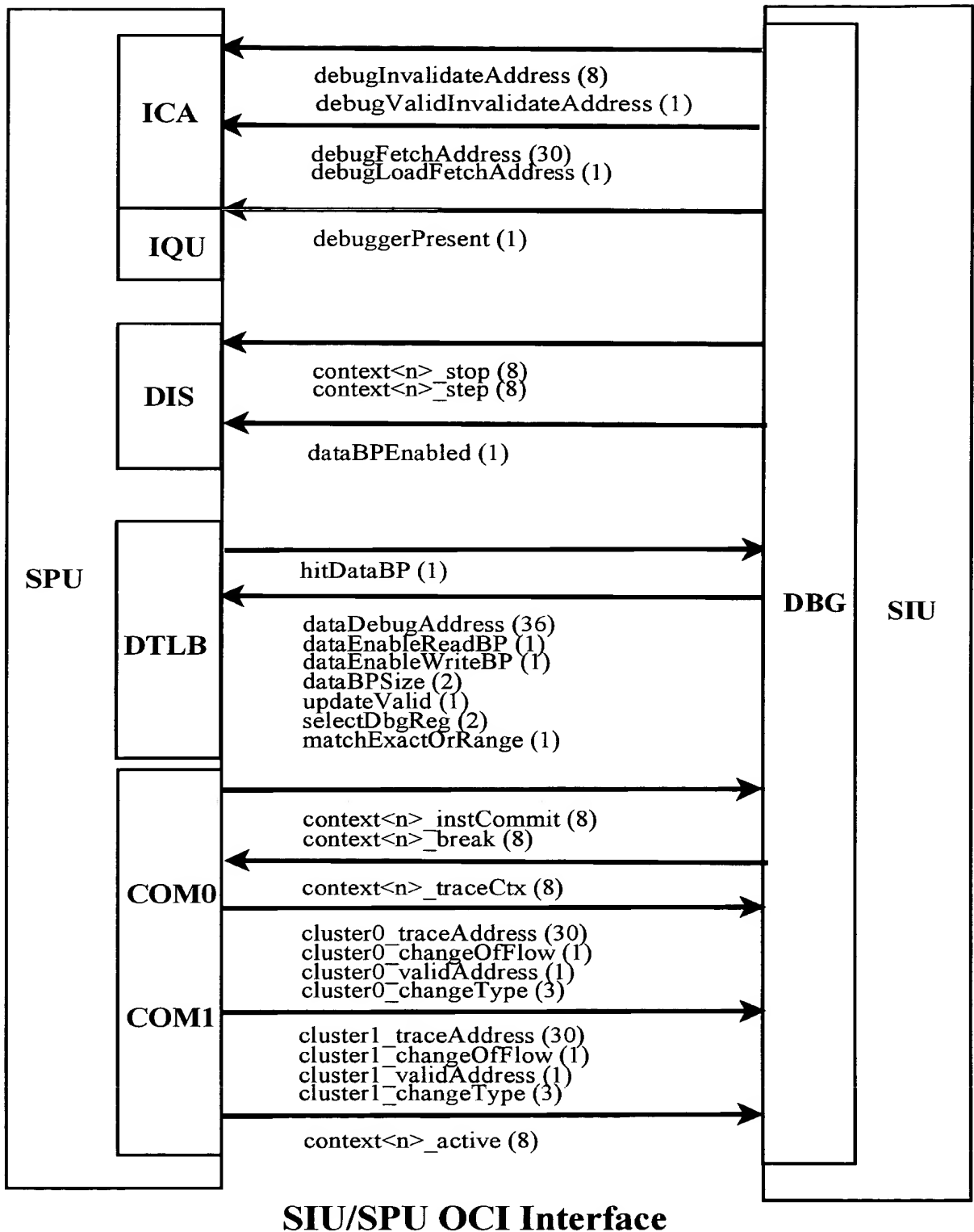
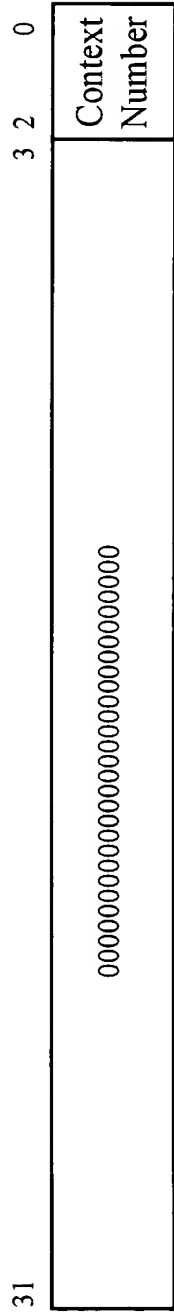


Fig. 22

Context Register



Context Number Register

Fig. 25

<u>Bit Value</u>	<u>Type</u>
000	Branch Not Taken
001	Branch Taken
010	JMP, ERET
011	Exception - TLB Refill
100	Exception - General Exception
101	Exception - Packet Load Exception
110	Exception - Extended Interrupt
111	Invalid

Fig. 28

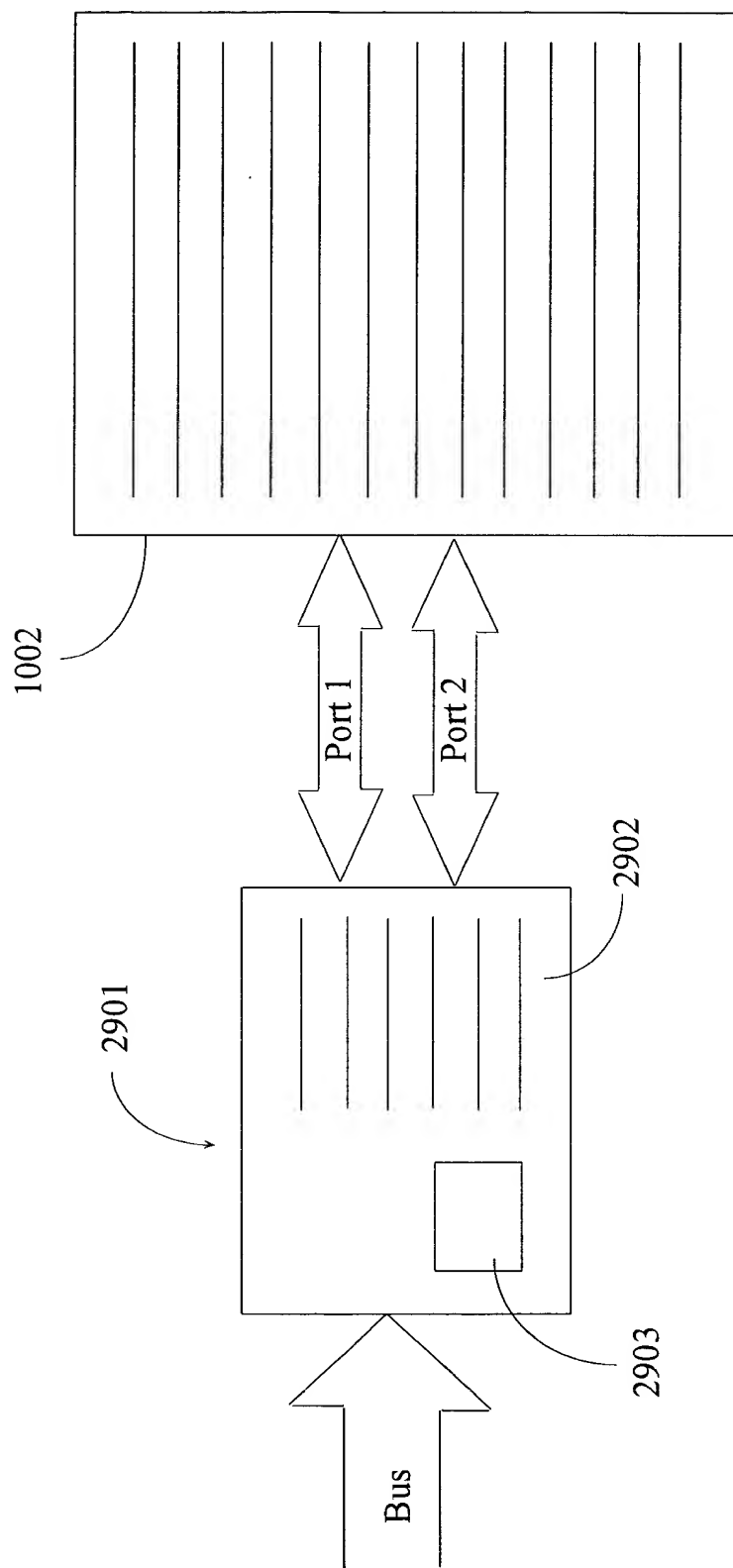


Fig. 29